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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,319	08/17/2001	Gerard Chauvel	TI-31357	5661

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	13

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,319	CHAUVEL, GERARD	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9,10,14,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,10,14,15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 January 2004 has been entered.

Claim Objections

2. Claims 14-15 and 17-18 are objected to because of the following informalities:

As per claim 14, line 14, --and does-- should be added after "field".

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-4, 9-10, 14-15, and 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant sets forth that the invalidate TLB entry command is not issued in response to write transactions (see claim 1, lines 18-19; claim 14, line 14; remarks at page 7, next to last full paragraph). However, in Applicant's specification, it appears that Applicant discloses issuing an invalidate command in response to a write operation. See paragraph 71 on page 27 of the specification. It is not clear where Applicant has support for not generating an invalidate command in response to a write operation.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 9-10, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason et al. (5,319,760) in view of Chang et al. (6,119,204).

As per claims 1 and 14, Mason et al. teaches a central processing system ("processor") which employs a translation buffer caching recently used page table entries ("TLB" or "storage circuitry"). See column 3, lines 55-56, and column 4, lines 41-44. With reference to figure 10, a

virtual address is received on a set of inputs to the TB 48 and a physical address is output through selector 92 ("set of outputs"). The system of Mason et al. is a multitasking system, where several processes may reside in memory at the same time ("executing a plurality of program tasks within the processor" and "initiating a plurality of memory access requests in response to the plurality of program tasks"). See column 9, lines 11-13. As set forth in column 4, lines 41-44, recently used page table entries are cached in the translation buffer ("caching a plurality of translated memory addresses in the TLB responsive to the plurality of memory access requests").

The page table entries stored in the translation buffers 36 and 48 include an address space number field ("task identification value"), or ASN. See column 9, lines 35-36 and 47-51. The address space number is loaded from the process control block (see column 9, lines 50-51) and therefore Mason et al. teaches that the ASN stored in the page table entries of the translation buffer "indicate which of the plurality of program tasks requested the respective translated memory address".

Mason et al. teaches that each page table entry 81 (figure 9) stores a bit called an "address space match" which allows the operating system to designate locations in the systems virtual address space which are shared among all processes ("incorporating a shared indicator with each translated memory address to indicate when a translated memory address is shared by more than one of the plurality of program tasks"). See column 11, line 65, to column 12, line 3.

Mason et al. further teaches flushing entries in the translation buffer when there is a context switch, where useful entries in the TB are not flushed (see column 9, lines 43-47) and the address space match bit ("shared indicator") is utilized determine if a particular entry should not

be flushed (i.e. invalidated) on a context switch ("in a manner qualified by the shared indicator"). See column 2, lines 38-44. It is noted that a context switch, where the present invalidation occurs, does not change data in any other memory (i.e. the invalidation does not occur in response to a write operation).

Mason et al. does not teach an invalidate TLB entry command to initiate the invalidation of the TLB entries. Chang et al. teaches that it was known to invalidate TLB entries on a context switch using an explicit TLB invalidate instruction. See column 1, lines 60-61 and 63-67. It would have been obvious to one of ordinary skill in the art to have utilized a TLB invalidate command to invalidate the entries in the translation buffer of Mason et al., as taught by Chang et al., because Chang et al. suggests that a TLB invalidate command is an efficient mechanism for initiating a TLB invalidation operation in software based coherency systems (see column 1, lines 64-66), such as the system of Mason et al., where the virtual memory system is managed by the operating system.

As per claims 3 and 18, Mason et al. teaches invalidating entries in the TB that match a particular address space number, where addresses that do not match the address space number are not flushed from the TB. See column 11, lines 57-61. Therefore, the combination of Mason et al. and Chang et al. teaches invalidating entries using an invalidation command where the address space number in the TB matches the address space number of the invalidate operation.

As per claim 9, Mason et al. teaches a set a page tables for generating a translated address stored in memory 12. See column 9, lines 55-65. Each page table entry (PTE) in the memory 12 includes 16 bits as set forth in Table A (column 15), including the "address space match" bit <4>. See column 9, lines 32-34.

As per claim 10, the combination of Mason et al. and Chang et al. does not teach not storing the address space match bit in the page translation tables. However it would have been obvious to one of ordinary skill in the art to have not included the address space match bit in the page translation tables because the status of a particular entry as being related to multiple tasks may change dynamically, and not storing information that may change quickly within the page tables would save memory, thereby reducing system cost.

7. Claims 2 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Mason et al. and Chang et al. in view of Bausch (6,339,816).

The combination of Mason et al. and Chang et al. does not teach invalidating shared TB entries. Bausch teaches that it was known in invalidate shared TLB entries on context switches to write protected pages (before any writes occur to a page). See column 2, lines 57-63, and column 3, lines 1-3. It is noted that Mason et al. teaches write protection information for individual pages at column 9, lines 19-25. It would have been obvious to have modified the combination of Mason et al. and Chang et al. such that shared pages are invalidated on context changes, where the pages had their write permission temporarily changed, because Bausch suggests that such a modification would permit efficient restoration of write protection during a context switch after changing the write protection for the benefit of correcting stored code or writing new code from the system side (see column 1, lines 43-45, and column 2, lines 61-62).

8. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Mason et al. and Chang et al. in view of Slater, "A Guide to RISC Microprocessors".

As per claims 4 and 15, the combination of Mason et al. and Chang et al. does not teach that the system has several levels of TLB and invalidating encompasses invalidating all of the levels of TLB. Slater teaches that it was known to include a "2nd" level of TLB, called the TLB slice, in addition to the traditional full TLB. See page 115. Slater also teaches that the TLB slice is updated along with the full TLB. See page 116, second full paragraph. It would have been obvious to one of ordinary skill in the art to have modified the combination of Mason et al. and Chang et al. to include a TLB slice as a second level of TLB, because Slater teaches that such an implementation would reduce the amount of transistors on the CPU chip.

Response to Arguments

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Conclusion

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
March 3, 2004